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MAGNETORESISTANCE MOBILITY PROFILING OF MESFET CHANNELS.(U)
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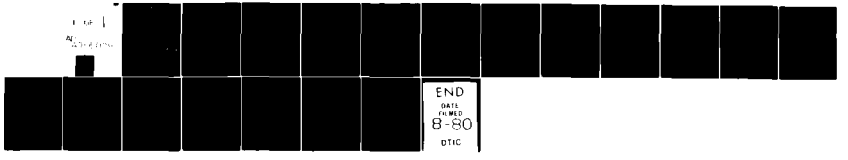

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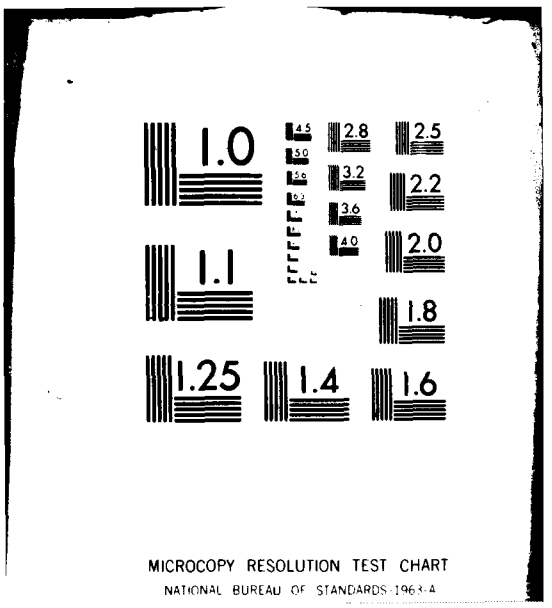
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Magnetoresistance provides a straightforward, non-destructive technique for determining the carrier mobility in the conducting channel of field effect transistors (FETs) over their full range of operation. The analysis is well suited to the typical FET geometry. The technique is illustrated here by a comparative study of GaAs depletion mode FET devices.

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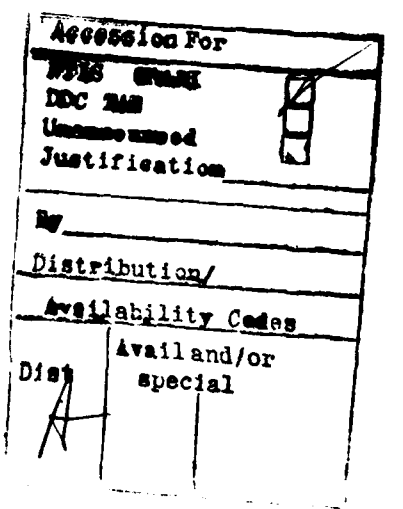
by
J. R. Sites
and
H. H. Wieder



Report SF27

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MAGNETORESISTANCE MOBILITY PROFILING OF MESFET CHANNELS

J. R. Sites and H. H. Wieder

ABSTRACT

Magnetoresistance provides a straightforward, non-destructive technique for determining the carrier mobility in the conducting channel of field-effect transistors (FETs) over their full range of operation. The analysis is well suited to the typical FET geometry. The technique is illustrated here by a comparative study of GaAs depletion-mode FET devices.

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I. INTRODUCTION

The carrier mobility in the conducting channel of a field-effect transistor (FET) will, in general, vary with the degree of conduction in the channel. In practical FETs the mobility is usually dependent on the chemical and metallurgical aspects of fabrication, in particular, the spatial distribution of various impurities and lattice defects, as well as the interaction between them. The specific thickness profiles of both electron density $n(x)$ and mobility $\mu(x)$ of a GaAs depletion-mode metal-semiconductor field-effect transistor (MESFET) may have a significant effect on its dynamic range of operation, its frequency response, and its noise characteristics. Clearly a quantitative evaluation of these profiles is important for improving and optimizing MESFET fabrication procedures.

One method for deriving the channel mobility profile utilizes the frequency dependence of the gate-source impedance of GaAs MESFET, as described by Lehovec.[1] The mobility profile is determined from a transmission line analysis of the frequency and voltage dependence of the gate-source capacitance and Q-factor. However, the experimental measurements are cumbersome and their interpretation is questionable in the vicinity of the interface between the n-type epitaxial layer and the semi-insulating GaAs substrate.

A different technique used for measuring $\mu(x)$ is described by Tansley.[2] He applied a step-wise adjusted reverse DC bias to the Schottky barrier gate of a cloverleaf-like structure such as described by van der Pauw[3] for resistivity and Hall effect measurements. The bias determines the depth of the depleted region under the gate. A small AC

signal superposed upon the DC bias provides for the characterization of a thin lamina of the channel. The mobility $\mu(x)$ is calculated from the Hall coefficient profile, $R_h(x)$, and the resistivity profile, $\rho(x)$. Disadvantages of this method are that it measures the Hall mobility rather than the drift mobility and that a special test structure is required. Thus the measurements cannot be performed on conventional MESFET.

A method of measuring the drift mobility profile was described by Pucel and Krumm.[4] It is based on a low-frequency evaluation of the bias dependence of the gate capacitance and transconductance, using for this purpose a special MESFET structure in which the gate length is made large enough to avoid fringing capacitance problems. Inaccuracies, however, may be introduced by series resistance effects under high-gate bias[5], and the special long-gate test structure does not give a direct comparison with the properties of a conventional MESFET.

A laborious but effective procedure used to determine $\mu(x)$ is a sequentially repeated[6] electrochemical anodization and etch-stripping of the anodized layer followed by electrical and galvanomagnetic measurements made on the residual portion of the n-type epitaxial layer. Jay *et al*[7] have compared the anodization etch-stripping method of measuring $\mu(x)$ with the Schottky barrier gated-cloverleaf and with the long-gate MESFET techniques. For this purpose, they used n-type epitaxial layers grown on a semi-insulating GaAs substrate with the intermediate high-resistivity undoped GaAs buffer layers between them. They found that the gated-cloverleaf method provides a higher spatial resolution of $\mu(x)$ than anodization and etch-stripping and

that the mobility determined by means of these methods is essentially constant and independent of position.

A method useful for determining $\mu(x)$ by means of gate-controlled magnetoresistance measurements made on specimens having Corbino disc circular symmetry was described by Poth.[8] Such Corbino discs were made of epitaxial n-type GaAs layers having coaxial circular central and peripheral ohmic contacts. An annular Schottky barrier gate was used to control the effective thickness of the conducting channel. In the absence of a magnetic field, the current density has radial symmetry. The current streamlines, however, become logarithmic spirals with a characteristic Hall angle θ in a transverse magnetic field B. Assuming, to first order, that the drift and magnetoresistance electron mobilities are the same, the magnetic field-dependent resistance R_B of the Corbino disc channel is

$$R_B = R_0(1 + \mu^2 B^2) \tag{1}$$

where R_0 is the resistance of the disc in zero magnetic field. The channel mobility is thus

$$\mu = \frac{1}{B}\,(R_B/R_0 - 1)^{\frac{1}{2}} \tag{2}$$

The electron mobility profile of GaAs Corbino discs calculated by means of Eqn. (2) from the gate-voltage dependence of the magnetoresistance measured experimentally by Poth was found to be in good agreement with theoretically expected values for different electron concentrations. However, such gated Corbino disc measurements require the specific configuration which is quite different from that of conventional MESFET structures and once again may not reflect the mobility profile of actual MESFETs.

An alternative and superior technique is to derive the channel mobility from magnetoresistance measurements made on conventional depletion-mode GaAs MESFET by taking account of the specific geometry of the conducting channel between source and drain whose length-to-width ratio, $\ell/w \ll 1$. Kuhrt and Lippmann[9] have calculated the magnetoresistance of a rectangular flat plate by conformal mapping procedures. For ℓ/w and $\mu B \lesssim 0.4$, they find

$$\frac{R_B}{R_o} = \frac{\rho_B}{\rho_o}\left[1 + \mu^2 B^2 (1 - 0.54\, \ell/w)\right] . \qquad (3)$$

The ratio ρ_B/ρ_o is the physical magnetoresistance, which would reflect a non-unity Hall factor resulting from an energy dependent scattering time.

II. EXPERIMENTAL RESULTS

We have used such a magnetoresistance mobility profiling technique on a variety of MESFETs made primarily of III-V compound semiconductors and intended for use in high frequency or microwave amplifiers. For exploratory purposes we used an 8T superconducting magnet with room temperature access, but for most applications a standard electromagnet with a peak magnetic field of the order of 1T is adequate. We present here the results of a comparative study of five GaAs depletion-mode MESFETs from different sources as shown in Table I. They were chosen as representative of different fabrication techniques. The conducting channels of the various MESFETs were grown either by liquid-phase epitaxy (LPE), by vapor-phase epitaxy (VPE) on a buffer layer, or by the ion implantation of donor atoms into semi-insulating GaAs. All of the devices have the same nominal carrier concentration, similar channel conductivities, and similar length-to-width ratios.

In all cases the magnetoresistance was found to have a quadratic dependence on magnetic field up to $\mu B \approx 1$. Figure 1(a) shows the magnetoresistance $(R_B/R_0 - 1)$ of a LPE-grown GaAs device (LPE-I). The Hall coefficient measured on a similarly grown, but thicker, layer processed into a Hall generator configuration with $\ell/w \approx 3$ is shown in Fig. 1(b). Within experimental uncertainty this Hall coefficient is constant up to 8T, which implies that for these n-type layers, the Hall factor is essentially unity, and therefore the Hall mobility and drift mobility can be considered to be the same. Since ℓ/w is ≈ 0.01 for all devices studies, Eqn. (3) thus reduces to Eqn. (2) to within a few percent.

In order to convert channel mobilities to a mobility profile, the gate-voltage (V_G) dependence of the depletion layer depth must be determined. The usual depletion layer approximation which presumes that the electron density is homogeneous throughout the epilayer may not be accurate, since, in general, there will be an electron density profile $n(x)$ as well as a mobility profile $\mu(x)$. We have determined the gate-voltage dependence of the reverse-biased capacitance of a Schottky barrier on the same LPE-grown GaAs epilayer used to make the MESFET. The depletion layer depth δ was calculated from the measured capacitance C at a particular gate-voltage

$$\delta(V_G) = \varepsilon_s A/C(V_G) \tag{4}$$

where $\varepsilon_s = 13.3\ \varepsilon_0$ is the dielectric constant of GaAs, and A is the area of the capacitor. The gate-voltage dependence of δ is shown in Fig. 2(a). For comparison, the depletion depth determined from the depletion layer approximation

$$\delta = \left[\frac{2\varepsilon_s\ (V_{bi} - V_G - kT/q}{qn}\right]^{\frac{1}{2}} \qquad (5)$$

is also shown. For this curve the built-in potential V_{bi} was taken to be 0.8 volt and the average carrier density n assumed to be 1.4×10^{17} cm^{-3}. For reference, the measured conductivity of device LPE-I is shown in Fig. 2(b). It gives an indication of the region considered to be relevant for the determination of depletion depth. Note that for this particular device, the two depletion depth curves agree until the channel conductance has fallen to about 1% of its original value.

The mobility deduced from the magnetoresistance data of all five GaAs MESFETs is presented in Fig. 3 as a function of gate voltage. As a guide to the reader, an approximate depletion depth scale, taken from Eqn. (5) is also indicated. To show where pinch-off occurs, we have taken the measured channel conductance G, such as shown in Fig. 2(b), and extracted the surface density of electrons in the conductive channel N_s as follows

$$N_s = \frac{G}{1 - R_s G}\,\frac{\ell/w}{q\mu} \quad [cm^{-2}] \qquad (6)$$

R_s is a series resistance resulting from that part of the channel not covered by the gate, and leads to the correction factor in the denominator. The channel surface density N_s is also shown in Fig. 3.

III. DISCUSSION

The salient features of Fig. 3 are that in all cases the channel mobility is relatively constant as the channel thickness is decreased. In the vicinity of pinch-off, however, all the mobilities decrease by 30 - 60%. The constancy of the mobility with channel thickness agrees with the Corbino

disc results of Poth[8] and with the Hall measurements of Jay *et al.*[7] In the latter case, the GaAs epilayer and transistor fabrication procedures are presumed similar to the Plessey device we studied (VPE-II), and the mobility magnitudes (4000 cm^2/V-sec) also show good agreement. The electron mobility of the Texas Instruments device (VPE-I) appears to have a shallow peak. The origin of this peak is not certain, but is likely due to deliberate impurity grading during the growth of the epilayer. Alternatively, it could be due to degradation of the mobility near the Schottky barrier produced during the deposition of the metal-gate electrode. The former explanation is favored because the slope of the surface carrier density curve (Fig. 3) decreases in magnitude as the channel thickness is decreased.

The decrease in mobility as the edge of the space-charge region approaches the metallurgical interface of the epilayer and a high-resistivity substrate or buffer layer may be due to electron scattering from interfacial defects or to enhanced compensation from the diffusion of Cr acceptors into the epilayer. The decrease appears to be less pronounced in the VPE buffer layer devices than in the LPE devices directly on the substrate. Kim *et al*,[10] using large gate transconductance/capacitance measurements also report a mobility decrease, in their case a much larger contrast between buffered and non-buffered epilayers. They also found that the region near the epilayer-substrate interface shows a high etch-pit density and poor crystalline quality, as well as a high degree of compensation. Earlier measurements with long gate FETs[4,7] which imply an increased mobility near pinch-off may suffer from the series resistance effect discussed in Section. I.

The data we have presented are not true profiles $\mu(x)$ defined at a specific point in space. They are a weighted average

$$\mu = \frac{\int_{\delta}^{d} \mu(x)\, n(x)\, dx}{\int_{\delta}^{d} n(x)\, dx} \tag{7}$$

which are actually fairly close to the actual profile so long as $\mu(x)$ is varying slowly compared to $n(x)$. A proper evaluation, however, requires a knowledge of $n(x)$, which can in principle be calculated from the slope of N plotted in Fig. 3

$$n(x) = \left.\frac{dN_s}{d\delta}\right|_{\delta=x} = \frac{dN_s}{dV_G} \Big/ \frac{d\delta}{dV_G} \tag{8}$$

Once again the critical point is the relationship between depletion depth and gate voltage. Approximate results can utilize either of the curves in Fig. 2(a), but quantitative profiling in the pinch-off region requires a reliable evaluation of δ vs. V_G. Thus, while gate voltage-dependent magnetoresistance measurement of channel mobility provides important advantages over other techniques, it also should be used with a certain degree of caution.

ACKNOWLEDGMENT

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TABLE I. GaAs Devices Studied

Designation	Source	Channel Fabrication	Buffer Layer	Dopant	Nominal Concentration	Gate Dimensions	Pinch-off Voltage
LPE-I	NOSC (test)	LPE	No	Sn	10^{17} cm^{-3}	2 x 380 μm	1.7 V
LPE-II	Hewlett-Packard (HFET1001)	LPE	No	Sn	10^{17}	1.2 x 230	1.8
VPE-I	Texas Instruments (test)	VPE	Yes	S	10^{17}	0.6 x 75	2.8
VPE-II	Plessey (GAT-4)	VPE	Yes	S	10^{17}	1.2 x 150	2 2
Implant	TRW (test)	Ion Implanted	No	Si	10^{17}	1.2 x 125	4.1

FIGURE CAPTIONS

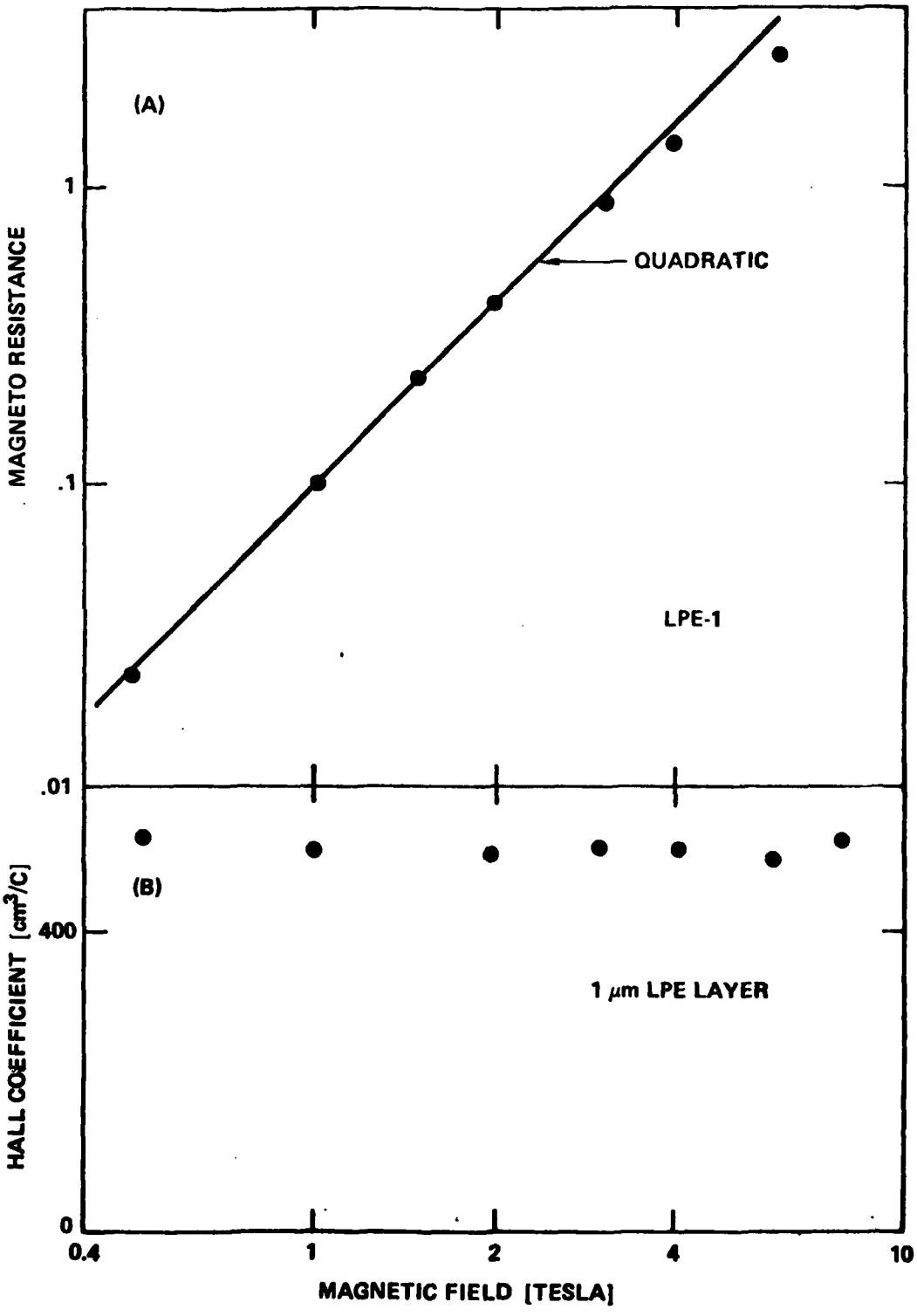
Figure 1. (a) Magnetoresistance of NOSC GaAs FET as a function of magnetic field; gate voltage = 0.

(b) Hall coefficient of similarly grown layer.

Figure 2. (a) Depletion depth δ as a function of gate voltage for NOSC LPE layers. Circles are from capacitance data, dashed line calculated from depletion approximation.

(b) Channel conductance of device made from this material.

Figure 3. Mobility (circles) and channel electron density (dots) vs. gate voltage for all five devices studied. Approximate distance scale shown for reference.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MAGNETO RESISTANCE
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LPE-1
.01
(B)
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HALL COEFFICIENT [cm³/C]
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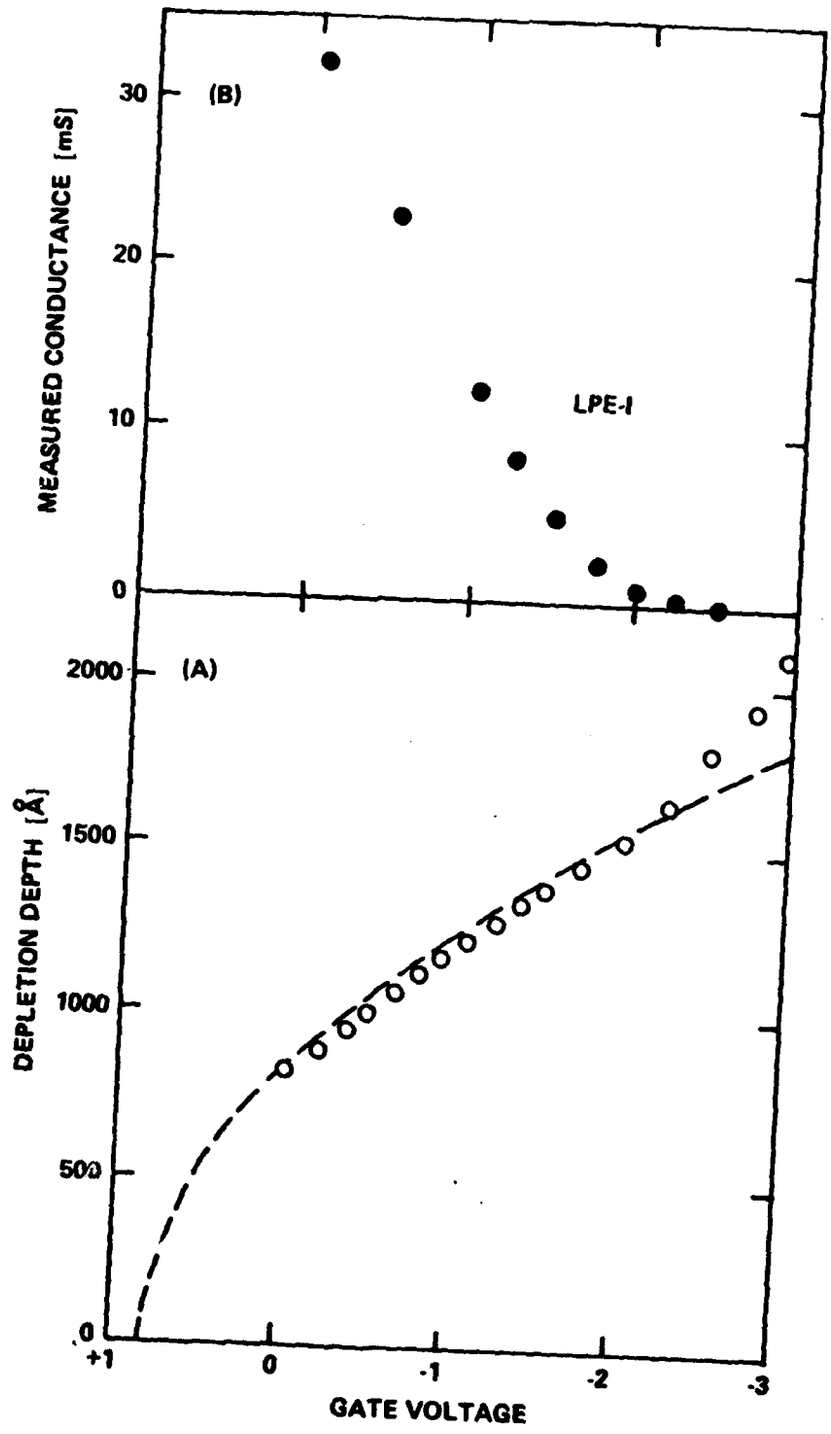
0.4
1
2
4
10
MAGNETIC FIELD [TESLA]

Fig. 1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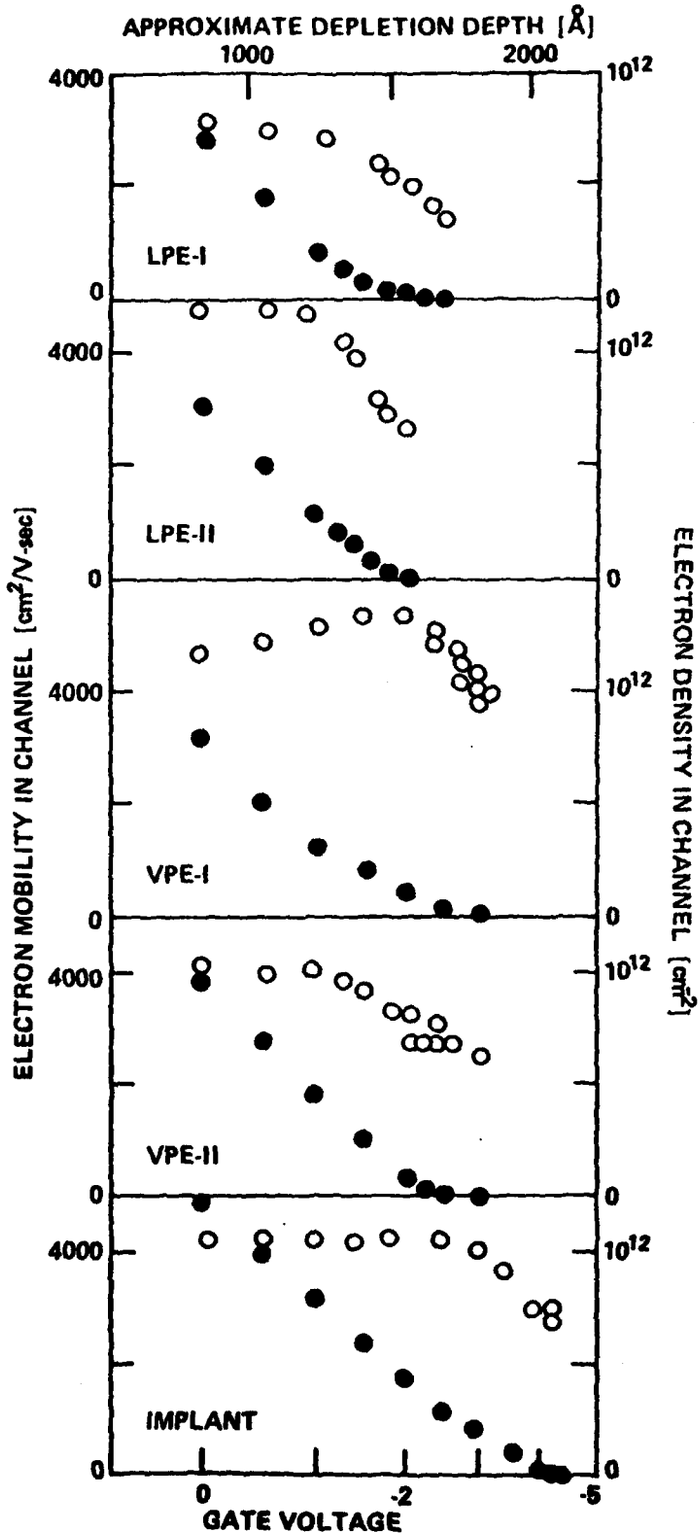
GATE VOLTAGE

Fig. 2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LPE-II
VPE-I
VPE-II
IMPLANT
ELECTRON MOBILITY IN CHANNEL [cm^2/V-sec]
ELECTRON DENSITY IN CHANNEL [cm^2]
0
-2
-5
GATE VOLTAGE

Fig. 3

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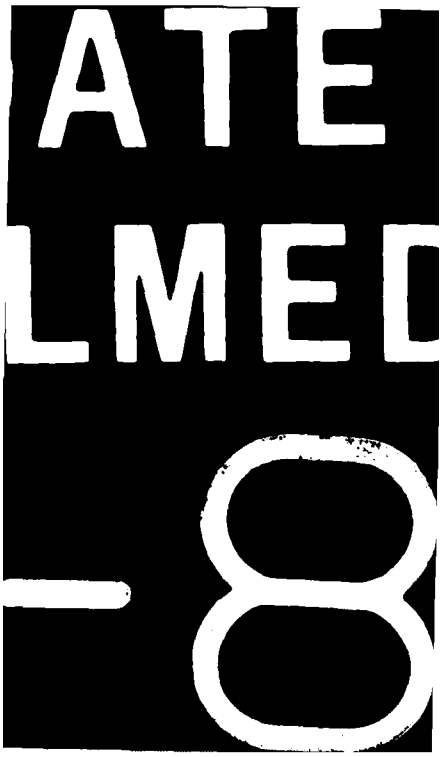
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